** San Francisco Bay University**

**EE461L - Verilog HDL Lab**

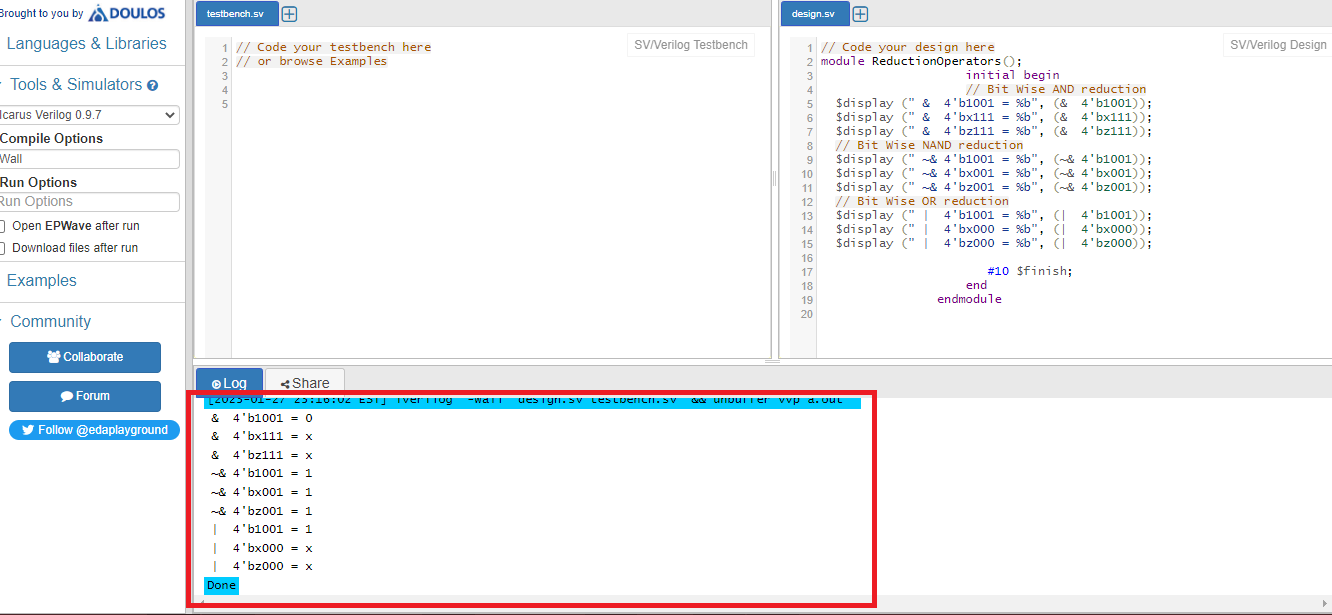
**Week#2 Verilog Language Concepts**

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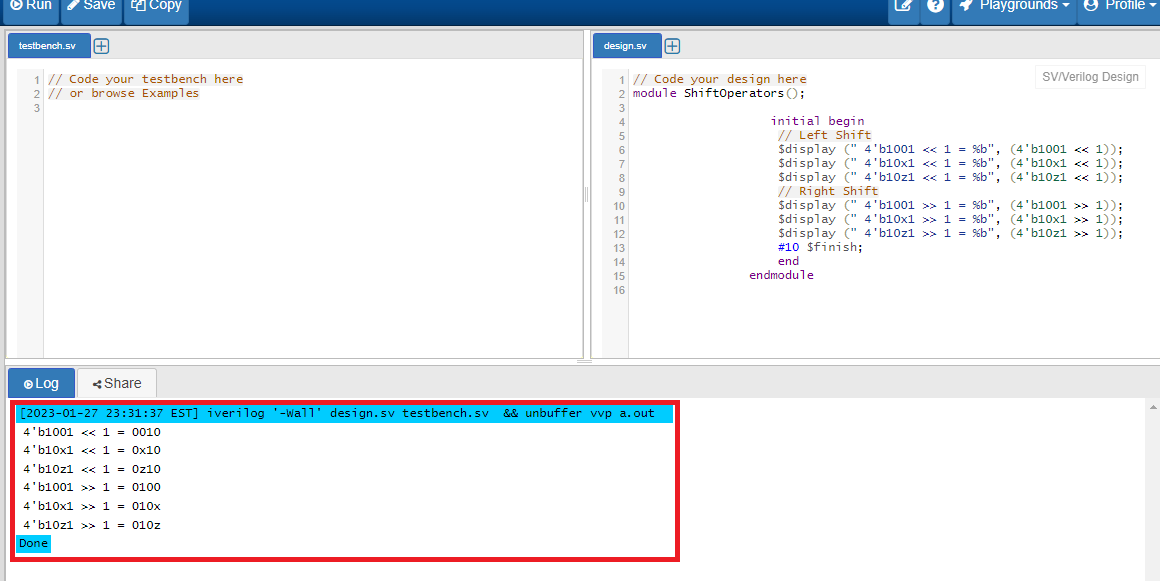
**Answers :**

1. Run module：

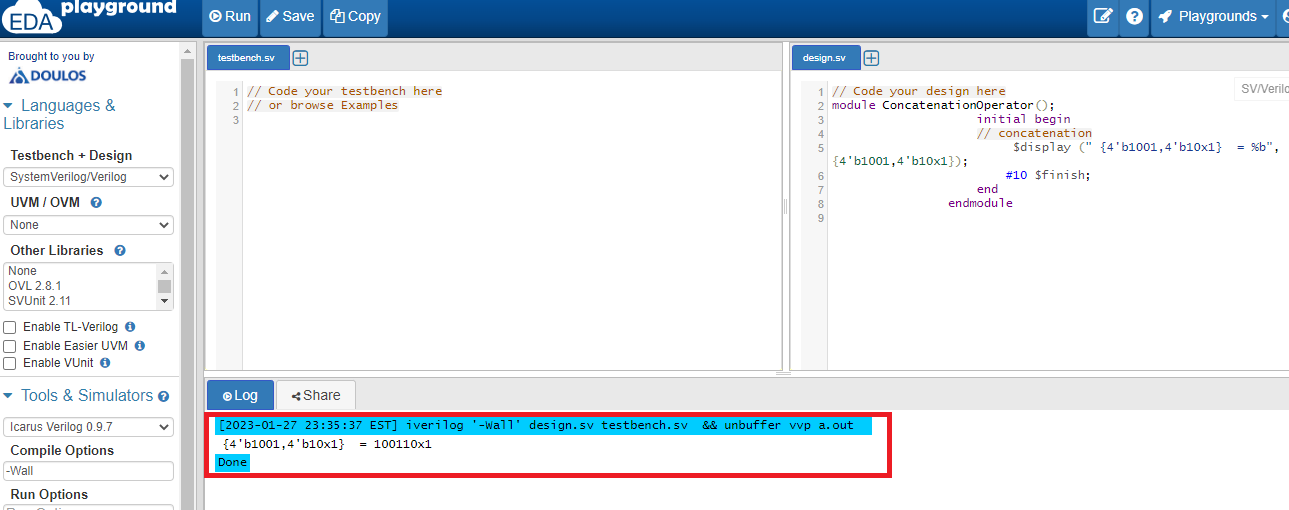
***Reduction Operators***



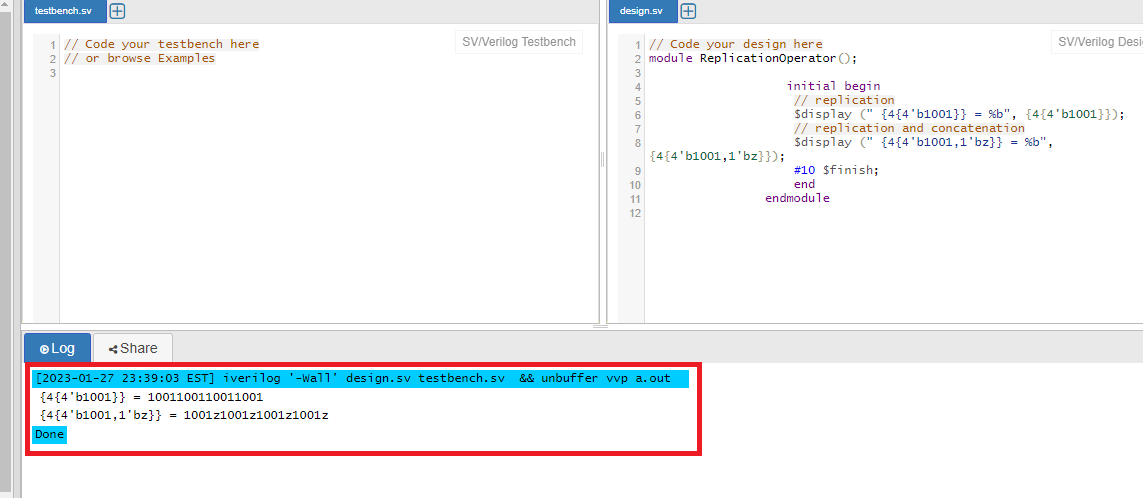
***Shift Operators***



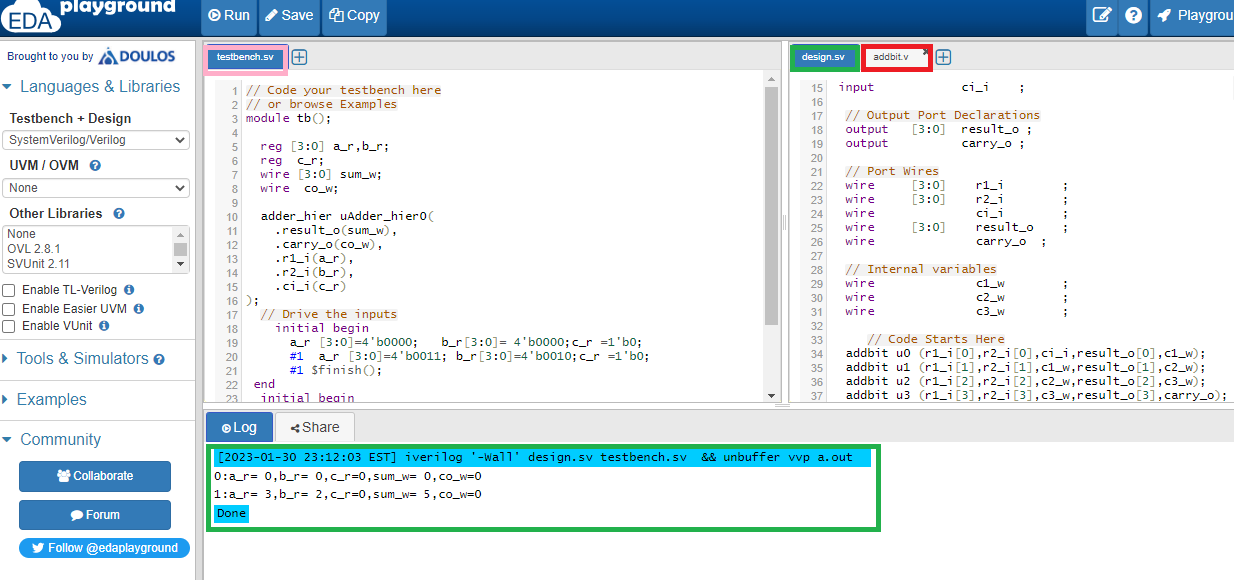
Concatenation Operator



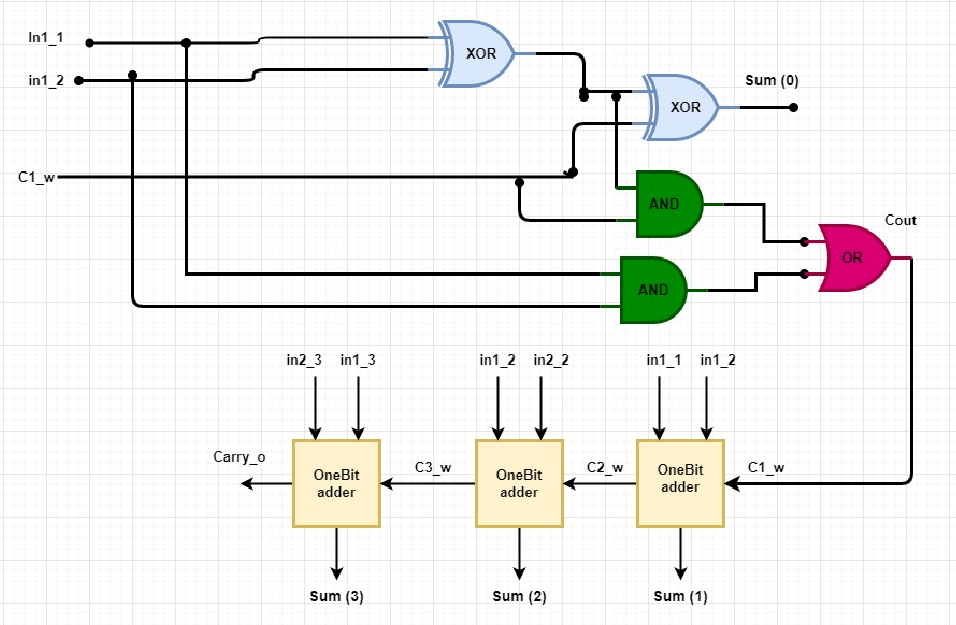
***Replication Operator***

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2. Complete the module addbit first, and then run module adder\_hier and its testbench.

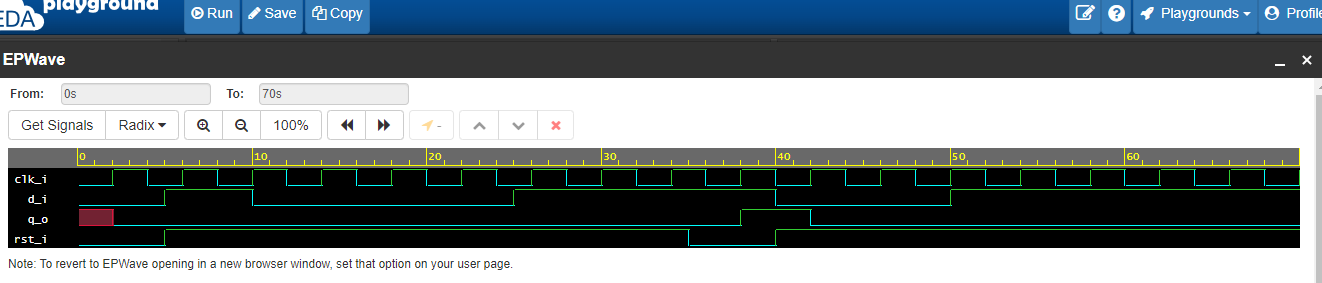


3. Based on the module adder\_hier, draw the circuit functional block diagram



4. Complete the testbenches for the modules DFFSynch, and DFFAsynch in Lab#1

DFFSynch



DFFAsynch

